LISTING OF CLAIMS

Please **amend** the claims as set forth below.

1. (currently amended) A method for fabricating a semiconductor device comprising:

forming a gate pattern and a source/drain region on a silicon substrate;

forming a Ni-based metal layer comprised of a nickel alloy for silicide on the silicon substrate where the gate pattern and the source/drain region are formed;

forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region; and

selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to expose a top portion of the nickel silicide on the gate pattern and the source/drain region,

whereby the nickel silicide on the gate pattern is neither shorted nor cut, and lumping of the nickel silicide is prevented, and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of one of Ta, Zr, Ti, Hf, W, Co, Pt, Pd, V, Nb, or any combination thereof.

2. (original) The method as claimed in claim 1, wherein the Ni-based metal layer for silicide is formed at a temperature of about 25 °C to about 500 °C.

3. (canceled)

4. (Canceled)

5. (original) The method as claimed in claim 1, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

6. (original) The method as claimed in claim 1, wherein the thermal treatment for forming the nickel silicide layer is carried out using a rapid thermal treatment system, a furnace, a sputter system, or any combination thereof.

7. (original) The method as claimed in claim 1, further comprises etching the silicon substrate using an RF sputter stching process to remove particles from the substrate after forming the source/drain.

8. (original) The method as claimed in claim 7, wherein the RF sputter etching process comprises forming the Ni-based metal layer for silicide and the N-rich titanium nitride layer in-situ.

Claims 9-11 (Canceled)

12. (currently amended) A method for fabricating a semiconductor device comprising:

forming a field region on a substrate to define an active region;

forming a gate pattern on the active region, wherein the gate pattern includes sidewalls;

forming spacers on the sidewalls of the gate pattern;

forming source/drain regions aligned with the spacers on both sides of the gate pattern;

cleaning the substrate using a wet cleaning process;

forming a Ni-based metal layer comprised of a nickel alloy for silicide on the entire surface of the substrate;

forming a N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region; and

cleaning the substrate to selectively to remove the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer and to expose a top portion of the nickel silicide layer formed on the gate pattern and the source/drain region.

whereby, the nickel silicide on the gate pattern is neither shorted nor cut, a pit is prevented from being formed in a boundary area between the active region and the field region, lumping of the nickel silicide is prevented, and a silicide residue is prevented from remaining on the spacers and the field region , and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of one of Ta, Zr, Ti, Hf, W, Co, Pt, Pd, V, Nb, or any combination thereof.

13. (original) The method as claimed in claim 12, wherein the Ni-based metal layer for silicide is formed at a temperature of about 25 °C to about 500 °C.

14. (canceled)

15. (Canceled)

16. (original) The method as claimed in claim 12, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

17. (original) The method as claimed in claim 12, wherein the thermal treatment for forming the nickel silicide layer is carried out using a rapid thermal treatment system, a furnace, a sputter system, or any combination thereof.

18. (original) The method as claimed in claim 12, further comprises etching the silicon substrate using an RF sputter etching process to remove particles from the substrate after forming the source/drain region.

19. (currently amended) A method for fabricating a semiconductor device comprising:

forming a gate pattern and a source/drain region on a silicon substrate;

forming a Ni-based metal layer comprised of a nickel alloy for silicide at a temperature of about 25 °C to about 500 °C on the silicon substrate where the gate pattern and the source/drain region are formed;

forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region; and

selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer, wherein a top portion of the nickel silicide on the gate pattern and the source/drain region is exposed , and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of one of Ta, Zr, Ti, Hf, W, Co, Pt, Pd, V, Nb, or any combination thereof.

20. (canceled)

21. (Canceled)

22. (Previously presented) The method as claimed in claim 19, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

23. (currently amended) A method for fabricating a semiconductor device comprising:

forming a field region on a substrate to define an active region;

forming a gate pattern on the active region, wherein the gate pattern includes sidewalls;

forming spacers on the sidewalls of the gate pattern;

forming source/drain regions aligned with the spacers on both sides of the gate pattern;

cleaning the substrate using a wet cleaning process;

etching the silicon substrate using an RF sputter etching process to remove particles from the substrate;

forming a Ni-based metal layer comprised of a nickel alloy for silicide on the entire surface of the substrate;

forming a N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region; and

cleaning the substrate to selectively to remove the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer and to expose a top portion of the nickel silicide layer formed on the gate pattern and the source/drain region exposed , and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of one of Ta, Zr, Ti, Hf, W, Co, Pt, Pd, V, Nb, or any combination thereof.

24. (canceled)

25. (canceled)

26. (currently amended) The method as claimed in claim 23 ~~26~~, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

Please **add** the following new claims:

27. (New) The method of claim 1, wherein the nickel alloy layer includes greater than 0 to about 20 % of one of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

28. (New) The method of claim 12, wherein the nickel alloy layer includes greater than 0 to about 20 % of one of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

29. (New) The method of claim 19, wherein the nickel alloy layer includes greater than 0 to about 20 % of one of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

30. (New) The method of claim 23, wherein the nickel alloy layer includes greater than 0 to about 20 % of one of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.